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| Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary) | | | | Complete if Known | |
| | | | | Application Number | 10/757,939 |
| | | | | Filing Date | January 16, 2004 |
| | | | | First Named Inventor | Craig C. HANSEN, et al. |
| | | | | Group Art Unit | 2183 |
| | | | | Examiner Name | CHAN, EDDIE P |
| Sheet | 1 | of | 10 | Attorney Docket Number | 43876-153 |

| U.S. PATENT DOCUMENTS | | | | | |
|-----------------------|-----------------------|--|--------------------------------|--|---|
| Examiner Initials* | Cite No. ¹ | Document Number | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
| | | Number-Kind Code ² (if known) | | | |
| 17 | AA | US-4,852,098 | 07/25/1989 | Brechard, et al. | |
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| | | Country Code ³ Number ⁴ Kind Code ⁵ (if known) | | | | |
| 15 | AT | WO 93/11500 | | | | |

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| OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS | | | |
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| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | T ² |
| H | AU | IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications and Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (Mar. 1992) (50006DOC018530 – 563) | |
| | AV | IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)," IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995) (50006DOC018413 – 529) | |
| | AW | Gerry Kane et al., "MIPS RISC Architecture," Prentice Hall (1995) (50006DOC018576 – 848) | |
| | AX | IBM, "The PowerPC Architecture: A Specification For A New Family of RISC Processors," 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994) (50006DOC019229 – 767) | |
| | AY | Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set," Manual Part No. 09740-90039, (1990) (50006DOC018849 – 19228) | |
| | AZ | MIPS Computer Systems, Inc., "MIPS R4000 User's Manual," Mfg. Part No. M8-00040, (1990) (50006DOC017026 – 621) | |
| | BA | i860™ Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn | |
| | BB | Gove, "The MVP: A Highly-Integrated Video Compression Chip," IEEE Data Compression Conference, pp. 215-24 (March 1994) (51056DOC000891 – 900) | |
| | BC | Gove, "The Multimedia Video Processor (MVP): A Chip Architecture for Advanced DSP Applications," IEEE DSP Workshop, pp. 27-30 (October 2-5, 1994) (51056DOC015452 – 455) | |
| | BD | Gutttag et al., "A Single-Chip Multiprocessor for Multimedia: The MVP," IEEE Computer Graphics & Applications, pp. 53-64 (November 1992) (51056DOC000913 – 924) | |
| | BE | Lee et al., "MediaStation 5000: Integrating Video and Audio," IEEE Multimedia pp. 50-61 (Summer 1994) (51056DOC000901 – 912) | |
| | BF | TMS320C80 (MVP) Parallel Processor User's Guide, Texas Instruments (March 1995) (51056DOC003744 – 4437) | |
| | BG | TMS320C80 (MVP) Master Processor User's Guide, Texas Instruments (March 1995) (51056DOC000925 – 957) | |
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| | BJ | Gwennap, "New PA-RISC Processor Decodes MPEG Video: Hewlett-Packard's PA-7100LC Uses New Instructions to Eliminate Decoder Chip," Microprocessor Report, pp. 16-17 (January 24, 1994) (51056DOC002140 – 141) | |
| BK | Gwennap, "Digital MIPS Add Multimedia Extensions," Microdesign Resources, pp. 24-28 (November 18, 1996) (51056DOC003454 – 459) | | |
| BL | Kurpanek et al., "PA7200: A PA-RISC Processor with Integrated High Performance MP Bus Interface," IEEE COMPCON '94, pp. 375-82 (February 28- March 4, 1994) (51056DOC002149 – 156) | | |
| BM | Lee et al., "Pathlength Reduction Features in the PA-RISC Architecture," IEEE COMPCON, pp. 129-35 (February 24-28, 1992) (51056DOC068161 – 167) | | |
| BN | Lee et al., "Real-Time Software MPEG Video Decoder on Multimedia-Enhanced PA 7100LC Processors," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 60-68 (April 1995) (51056DOC013549 – 557) | | |

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| FOREIGN PATENT DOCUMENTS | | | | | | |
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| Examiner Initials* | Cite No. ¹ | Foreign Patent Document | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear | T ⁶ |
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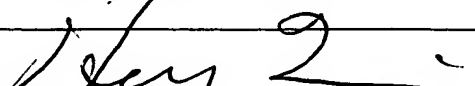
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| OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS | | | |
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| Examiner Initials | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | T ² |
|  | BX | Lee, "Realtime MPEG Video via Software Decompression on a PA-RISC Processor," IEEE, pp. 186-92 (1995) (51056DOC007345 - 351) | |
| | BY | Martin, "An Integrated Graphics Accelerator for a Low-Cost Multimedia Workstation," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 43-50 (April 1995) (51056DOC072083 - 090) | |
| | BZ | Undy et al., "A Low-Cost Graphics and Multimedia Workstation Chip Set," IEEE Micro, pp. 10-22 (April 1994) (51056DOC002578 - 590) | |
| | CA | HP 9000 Series 700 Workstations Technical Reference Manual: Model 712, Hewlett-Packard (January 1994) (51056DOC068048 - 141) | |
| | CB | PA-RISC 1.1 Architecture and Instruction Set Reference Manual, Third Edition, Hewlett-Packard (February 1994) (51056DOC002157 - 176) | |
| | CC | Ang, "StarT Next Generation: Integrating Global Caches and Dataflow Architecture," Proceedings of the ISCA 1992 Dataflow Workshop (1992) (51056DOC071743 - 776) | |
| | CD | Beckerle, "Overview of the StarT (*T) Multithreaded Computer," IEEE COMPCON '93, pp. 148-56 (February 22-26, 1993) (51056DOC002511 - 519) | |
| | CE | Diefendorff et al., "The Motorola 88110 Superscalar RISC Microprocessor," IEEE pp. 157-62 (1992) (51056DOC008746 - 751) | |
| | CF | Gipper, "Designing Systems for Flexibility, Functionality, and Performance with the 88110 Symmetric Superscalar Microprocessor," IEEE (1992) (51056DOC008758 - 763) | |
| | CG | Nikhil et al., "T: A Multithreaded Massively Parallel Architecture," Computation Structures Group Memo 325-2, Laboratory for Computer Science, Massachusetts Institute of Technology (March 5, 1992) (51056DOC002464 - 476) | |
| | CH | Papadopoulos et al., "T: Integrated Building Blocks for Parallel Computing," ACM, pp. 624-35 (1993) (51056DOC007278 - 289) | |
| | CI | Patterson, "Motorola Announces First High Performance Single Board Computer Using Superscalar Chip," Motorola Computer Group (Sept. 1992) (51056DOC069260 - 262) | |
| | CJ | M. Phillip, "Performance Issues for 88110 RISC Microprocessor," IEEE, 1992 (51056DOC008752 - 757) | |
| | CK | M. Smotherman et al., "Instruction Scheduling for the Motorola 88110," IEEE, 1993 (51056DOC008784 - 789) | |
| | CL | R. Mueller, "The MC88110 Instruction Sequencer," Northcon, 1992 (51056DOC009735 - 738) | |
| | CM | J. Arends, "88110: Memory System and Bus Interface," Northcon, 1992 (51056DOC009739 - 742) | |
| | CN | K. Pepe, "The MC88110's High Performance Load/Store Unit," Northcon, 1992 (51056DOC009743 - 747) | |
| | CO | J. Maguire, "MC88110: Datpath," Northcon, 1992 (51056DOC010059 - 063) | |
| | CP | Abel et al., "Extensions to FORTRAN for Array Processing," ILLIAC IV Document No. 235, Department of Computer Science, University of Illinois at Urbana-Champaign (September 1, 1970) (51056DOC001630 - 646) | |
| | CQ | Barnes et al., "The ILLIAC IV Computer," IEEE Transactions on Computers, Vol. C-17, No. 8, pp. 746-57 (August 1968) (51056DOC012650 - 661) | |
| CR | Knapp et al., "Bulk Storage Applications in the ILLIAC IV System," ILLIAC IV Document No. 250, Center for Advanced Computation, University of Illinois at Urbana-Champaign (August 3, 1971) (51056DOC001647 - 656) | | |
| CS | Awaga et al., "The μ VP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation," IEEE Micro, Vol. 13, No. 5, pp. 24-36 (October 1993) (51056DOC011921 - 934) | | |
| CT | Takahashi et al., "A 289 MFLOPS Single Chip Vector Processing Unit," The Institute of Electronics, Information, and Communication Engineers Technical Research Report, pp. 17-22 (May 28, 1992) (51056DOC009798 - 812) | | |

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|  | CU | Uchiyama et al., "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," IEEE Micro (October 1993) (51056DOC000185 - 194) | | | |
| | CV | Broughton et al., "The S-1 Project: Top-End Computer Systems for National Security Applications," (October 24, 1985) (51056DOC057368 - 607) | | | |
| | CW | Farmwald et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291) | | | |
| | CX | Farmwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 - 034) | | | |
| | CY | Gilbert, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 - 279) | | | |
| | CZ | Widdoes, "The S-1 Project: Developing High-Performance Digital Computers," IEEE Computer Society COMPCON Spring 1980 (December 11, 1979) (51056DOC071574 - 585) | | | |
| | DA | Cornell, S-1 Uniprocessor Architecture SMA-4 (51056DOC056505 - 895) | | | |
| | DB | The S-1 Project, January 1985, S-1 Technical Staff (51056DOC057368 - 607) | | | |
| | DC | S-1 Architecture and Assembler SMA-4 Manual, December 19, 1979 (Preliminary Version) (51056DOC057608 - 918) | | | |
| | DD | Michielse, "Performing the Convex Exemplar Series SPP System," Proceedings of Parallel Scientific Computing, First Intl Workshop, PARA '94, pp. 375-82 (June 20-23, 1994) (51056DOC020754 - 758) | | | |
| | DE | Wadleigh et al., "High Performance FFT Algorithms for the Convex C4/XA Supercomputer," Poster, Conference on Supercomputing, Washington, D.C. (November 1994) (51056DOC068618) | | | |
| | DF | C4 Technical Overview (September 23, 1993) (51056DOC017111 - 157) | | | |
| | DG | Saturn Assembly Level Performance Tuning Guide (January 1, 1994) (51056DOC017369 - 376) | | | |
| | DH | Saturn Differences from C Series (February 6, 1994) (51056DOC017150 - 157) | | | |
| | DI | "Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390) | | | |
| | DJ | Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993) | | | |
| | DK | Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598) | | | |
| | DL | Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236) | | | |
| | DM | Saturn Overview (November 12, 1993) (51056DOC017111 - 157) | | | |
| DN | Convex Notebook containing various "Machine Descriptions" (51056DOC016994 - 7510) | | | | |
| DO | "Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383) | | | | |
| DP | Excerpt from Convex C4600 Assembly Language Manual, 1995 (51056DOC061441 - 443) | | | | |
| DQ | Excerpt from "Advanced Computer Architectures - A Design Space Approach," Chapter 14.8, "The Convex C4/XA System" (51056DOC061453 - 459) | | | | |
| DR | Convex C4600 Assembly Language Manual, First Edition, May 1995 (51056DOC064728 - 5299) | | | | |
| DS | Alvarez et al., "A 450MHz PowerPC Microprocessor with Enhanced Instruction Set and Copper Interconnect," ISSCC (February 1999) (51056DOC071393 - 394) | | | | |
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|--------------------|-----------|---|----|
| DT | | Tyler et al., "AltiVec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042) | |
| DU | | AltiVec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392) | |
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| EL | | N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551) | |
| EM | | N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509) | |
| EN | | N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441) | |
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| Examiner Signature | | Dated Considered | 4/10/06 |
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| | | | | Application Number | 10/757,939 |
| | | | | Filing Date | January 16, 2004 |
| | | | | First Named Inventor | Craig C. HANSEN, et al. |
| | | | | Group Art Unit | 2183 |
| | | | | Examiner Name | CHAN, EDDIE P |
| Sheet | 7 | of | 10 | Attorney Docket Number | 43876-153 |


| OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS | | | | |
|---|---|---|------------------|---------|
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS); title of the article (when appropriate); title of the item (book, magazine, journal, serial, symposium, catalog, etc); date, page(s), volume-issued number(s), publisher, city and/or country where published. | T ² | |
| 125 | ES | Amould et al., "The Design of Nectar: A Network Backplane for Heterogeneous Multicomputers," ACM (1989) (51056DOC020947 – 958) | | |
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| | PH | Lawrie, "Access and Alignment of Data in an Array Processor," IEEE Transactions on Computers, Vol. C-24, No. 12, pp. 99-109 (December 1975) (51056DOC002932 – 942) | | |
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| Examiner Signature | | | Dated Considered | 4/10/06 |

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450. If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

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| | | | | First Named Inventor | Craig C. HANSEN, et al. |
| | | | | Group Art Unit | 2183 |
| | | | | Examiner Name | CHAN, EDDIE P |
| Sheet | 8 | of | 10 | Attorney Docket Number | 43876-153 |

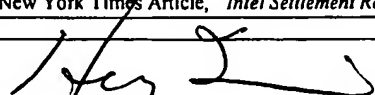
| OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS | | | | |
|---|-----------------------|---|----------------|--|
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS); title of the article (when appropriate); title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | T ² | |
| AS | FN | Rohrbacher et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp. 54-59 (August 1977) (reprinted version pp. 119-124) (51056DOC002943 - 948) | | |
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| | FQ | Singh et al., "A Programmable HIPPI Interface for a Graphics Supercomputer," ACM (1993) (51056DOC020888 - 896) | | |
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| | FW | Tullsen et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proceedings of the 22nd Annual International Symposium on Computer Architecture (June 1995) (51056DOC071434 - 443) | | |
| | FX | Turcotte, "A Survey of Software Environments for Exploiting Networked Computing Resources," Engineering Research Center for Computational Field Simulation (June 11, 1993) (51056DOC069098 - 256) | | |
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| | GA | Ware et al., "64 Bit Monolithic Floating Point Processors," IEEE Journal of Solid-State Circuits, Vol. Sc-17, No. 5 (October 1982) (51056DOC059646 - 655) | | |
| | GB | "Bit Manipulator," IBM Technical Disclosure Bulletin, pp. 1575-76 (November 1974) (51056DOC010205 - 206) | | |
| | GC | Finney et al., "Using a Common Barrel Shifter for Operand Normalization, Operand Alignment and Operand Unpack and Pack in Floating Point," IBM Technical Disclosure Bulletin, pp. 699-701 (July 1986) (51056DOC010207 - 209) | | |
| | GD | Data General AViiON AV500, 550, 4500 and 5500 Servers | | |
| | GE | Jovanovic et al., "Computational Science: Advances Through Collaboration," San Diego Supercomputer Center Science Report (1993) (51056DOC068769 - 779) | | |
| | GF | High Performance Computing and Communications: Toward a National Information Infrastructure, National Science Foundation (NSF) (1994) (51056DOC068791 - 801) | | |
| | GG | National Coordination Office for High Performance Computing and Communications, "High Performance Computing and Communications: Foundation for America's Information Future" (1996) (51056DOC072102 - 243) | | |
| AS | GH | Wilson, "The History of the Development of Parallel Computing," http://ei.cs.vt.edu/~history/Parallel.html (51056DOC068720 - 757) | | |

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| Examiner Signature |  | Dated Considered | 4/10/06 |
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| | | | | First Named Inventor | Craig C. HANSEN, et al. |
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| | | | | Examiner Name | CHAN, EDDIE P |
| Sheet | 9 | of | 10 | Attorney Docket Number | 43876-153 |

| OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS | | | | | |
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| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | T ² | | |
| | GI | IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (51056DOC019304 - 323) | | | |
| | | Original Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004 | | | |
| | GJ | Amended Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004 | | | |
| | GK | Expert Witness Report of Richard A. Killworth, Esq., <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005 | | | |
| | GL | Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005 | | | |
| | GM | Corrected Expert Report of Dr. Stephen B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-I; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005 | | | |
| | GN | Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005 | | | |
| | GO | Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005 | | | |
| | GP | Request for <i>Inter Partes</i> Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005 | | | |
| | GQ | Deposition of Larry Mennemeier on September 22, 2005 and Exhibit 501; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division | | | |
| | GR | Deposition of Leslie Kohn on September 22, 2005; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division | | | |
| | GS | Intel Article, "Intel Announces Record Revenue of 9.96 Billion", October 18, 2005 | | | |
| | GT | The New York Times Article, "Intel Posts 5% Profit Increase on Demand for Notebook Chips", October 19, 2005 | | | |
| | GU | USA Today Article, "Intel's Revenue Grew 18% In Robust Quarter for Tech", October 19, 2005 | | | |
| | GV | The Wall Street Journal Article, "Intel Says Chip Demand May Slow", October 19, 2005 | | | |
| | GW | The New York Times Article, "Intel Settlement Revives A Fading Chip Designer", October 20, 2005 | | | |
| Examiner Signature |  | | | Dated Considered | 4/10/06 |

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| INFORMATION DISCLOSURE CITATION IN AN APPLICATION | | | | ATTY. DOCKET NO. 043876-0153 | | SERIAL NO. 10/757,939 | | |
|---|----------|---|--------------------------------|---|---|---------------------------------|--|--|
| (PTO-1449) | | | | APPLICANT Craig HANSEN, et al. | | | | |
| | | | | FILING DATE January 16, 2004 | | GROUP 2183 | | |
| U.S. PATENT DOCUMENTS | | | | | | | | |
| EXAMINER'S INITIALS | CITE NO. | Document Number Number-Kind Code ² (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear | | | |
| | A | US 6,643,785 | 11-04-2003 | Hansen et al. | | | | |
| | B | US 6,725,356 | 04-20-2004 | Hansen et al. | | | | |
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| EXAMINER'S INITIALS | CITE NO. | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | | | | | | |
| | C | MARKOFF, JOHN, "Intel Settlement Revives a Fading Chip Designer," The New York Times (10-20-2005) | | | | | | |
| | D | Intel Press Release, "Intel Announces Record Revenue of \$9.96 Billion," Santa Clara, CA, 10-18-2005 | | | | | | |
| | | | | | | | | |
| EXAMINER | | | | DATE CONSIDERED 4/10/06 | | | | |

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SHEET 1 OF 11

INFORMATION DISCLOSURE
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APPLICATION

(PTO-1449)

ATTY. DOCKET NO.
043876-0153SERIAL NO.
10/757,939APPLICANT
HANSEN, C., et al.FILING DATE
January 16, 2004GROUP
2183

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| EXAMINER'S INITIALS | CITE NO. | Document Number Number-Kind Code ² (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|---------------------|----------|---|--------------------------------|---|---|
| 187 | | US 4,658,349 A | 05/14/1987 | Gafken | |
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

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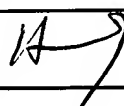
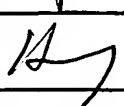
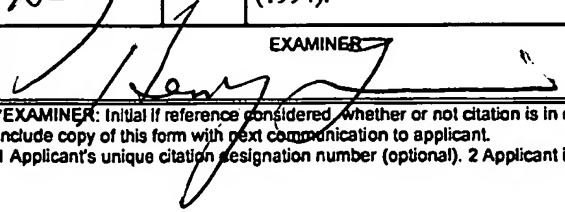
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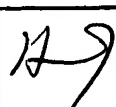

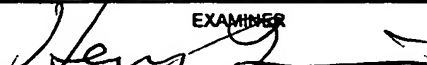
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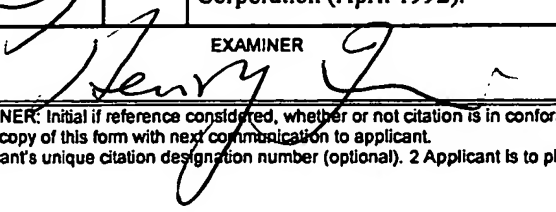
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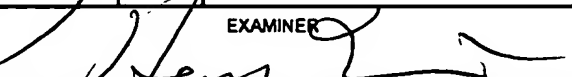
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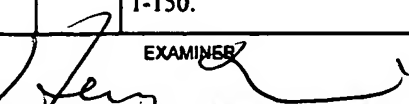
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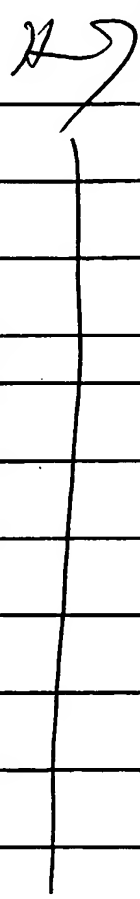
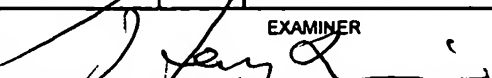
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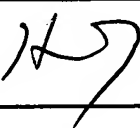
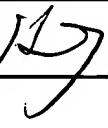

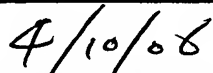
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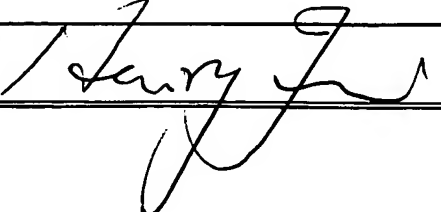
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